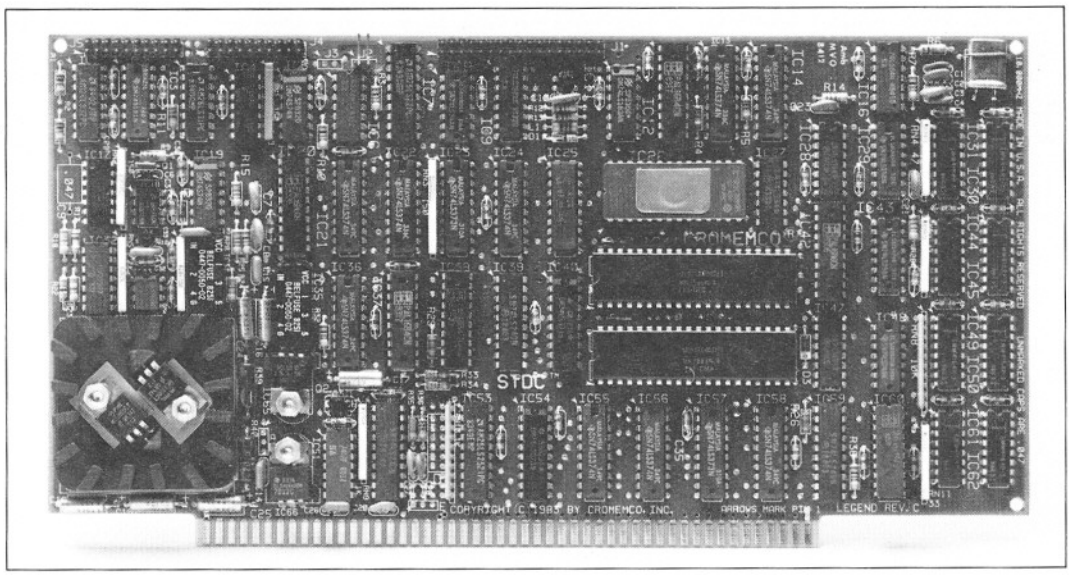
MODEL STDC
Intelligent ST-506 Winchester Disk Controller



FEATURES

- Industry's fastest ST-506 controller
- Supports two "ST-506" interface drives
- Five full-track cache memory
- Stores 10K bytes per track
- Read-after-Write verification
- Supports multiple logical drives
- DMA into 16 MB host address space
- Analog PLL, Write Precomp, CRC error check
- Power-fail write safeguard

PRODUCT DESCRIPTION

The STDC Disk Controller is a high-performance, highly flexible controller for 5-1/4" Winchester hard disks. An on-board Z80A microprocessor oversees the functions of the controller, including drive selection, head positioning, data buffer management, and error recovery. Since the STDC uses the ST-506 interface standard, provision has been made to support a wide variety of hard disk drives via programmable drive attributes and downloadable driver software. The STDC can support drives having up to 16 heads and 1024 cylinders, using either buffered or non-buffered seek protocols.

As an intelligent disk controller, the STDC needs minimal attention from the host operating system. The STDC fetches requests from the operating system through high speed access to main memory (DMA), performs the requested operation, Direct Memory Accesses the data back to the host memory, then interrupts the host to signal completion of the task. The host CPU, freed from the details of the disk access, may continue to execute instructions while the I/O operation is in progress, thus relieving the disk I/O bottleneck which constricts many multi-user systems.

The STDC further enhances the performance of sophisticated systems through use of five full-tracks of cache memory. This includes one dedicated verify buffer which is used to verify data after it is written to the disk. When a sector is requested by the operating system, that sector and all the other sectors on that track are read into one of the track buffers. The desired sector is then transferred to main memory, while the remaining sectors are retained inside the STDC until called for later by the operating system. When a new sector is requested, it can be delivered immediately, as can the next, and the next, and so on until the end of the track is reached. These caches of data appear to come from a very high speed disk drive.

The use of four full-tracks of cache memory allows the STDC to reserve separate caches for several users or processes, or for "source" and "destination" data in transfer operations. The four buffers may serve as read, write, or verify buffers as required by current conditions. If all four buffers are in use when a new operation is requested, the on-board Z80A determines which buffer can be freed; the buffer with the Least Recently Used (LRU) data is then selected for use in the new operation and the old data is either purged or written back to the disk as required. The STDC determines the LRU data from the frequency with which each buffer has been accessed and the time interval since the last access.

Another advanced capability of the STDC is a mode in which a single drive may be divided into a number of smaller logical units. As many as 32 units may be allocated on one physical drive. This feature allows users to have separate "drives," and allows the apparent size of the disk to be matched to the size of the backup medium if desired.

Other capabilities of the board include clock recovery via an on-board phase-locked loop, write data precompensation, and full formatting ability. The board generates and checks a cyclic redundancy code for all disk data, and automatically performs a read-after-write sequence to verify proper data transfer.

The power-fail write safeguard feature ensures that during a power failure no data is written to the drive.

TECHNICAL SPECIFICATIONS

Disk Interface:
ST-506

Drives Supported:
2

Actuators Supported:
Voice Coil (Buffered)
Stepper (Buffered)
Stepper (Unbuffered)

Disk Transfer Rate:
5 Megabits/sec

Storage per Track:
10K bytes

Cache Memory:
4 Read/Write tracks, 1 Write verify track

Cache Size:
10K bytes/track; 50K bytes total

DMA:
Disk-Data buffer at 1.6 μsec/byte
Data buffer-Main memory at 1.25 μsec/byte

S-100 Interrupts:
Vectored interrupt with priority controller

S-100 I/O Ports:
1 input, 1 output

Processor Type:
Z80A

Memory Complement:
64K bytes RAM
8K bytes ROM

Power Requirements:
+ 8 Volts at 2 Amps
+ 18 Volts at 50 milliamps
– 18 Volts at 50 milliamps

Operating Environment:
0–55 degrees Centigrade

Bus Interface:
IEEE-696 (S-100)

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